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Inventor Name Search Result

Your Search was:

Last Name = MOLL
First Name = LAURENT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11543549	Not Issued	41	10/04/2006	Cache instructions with hierarchy control	MOLL, LAURENT R.
11543598	Not Issued	94	10/04/2006	CACHE OPERATIONS WITH HIERARCHY CONTROL	MOLL, LAURENT R.
11559069	Not Issued	30	11/13/2006	SMALL AND POWER-EFFICIENT CACHE THAT CAN PROVIDE DATA FOR BACKGROUND DMA DEVICES WHILE THE PROCESSOR IS IN A LOW-POWER STATE	MOLL, LAURENT R.
11559133	Not Issued	30	11/13/2006	POWER CONSERVATION VIA DRAM ACCESS REDUCTION	MOLL, LAURENT R.
11559192	Not Issued	20	11/13/2006	POWER CONSERVATION VIA DRAM ACCESS	MOLL, LAURENT R.
11717511	7424561	150	03/13/2007	SYSTEMS USING MIX OF PACKET, COHERENT, AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS	MOLL, LAURENT R.
11740892	7443759	150	04/26/2007	REDUCED-POWER MEMORY WITH PER-SECTOR GROUND CONTROL	MOLL, LAURENT R.
11740901	Not Issued	30	04/26/2007	Reduced-Power Memory with Per-Sector Power/Ground Control and Early Address	MOLL, LAURENT R.
11751949	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY ENABLING LOW-POWER MODES	MOLL, LAURENT R.
11751973	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY ENABLING ALTERNATIVE OPERATIONAL MODES	MOLL, LAURENT R.
11751985	Not Issued	30	05/22/2007	RE-FETCHING CACHE MEMORY HAVING COHERENT RE-FETCHING	MOLL, LAURENT R.
11759216	Not Issued	25	06/06/2007	Software-Directed Rank Coalescing	MOLL, LAURENT R.

11759217	Not Issued	30	06/06/2007	Physical Memory Allocating According to Ranks	MOLL, LAURENT R.
11759218	Not Issued	30	06/06/2007	Associative Structure Rank Counters	MOLL, LAURENT R.
11803637	Not Issued	30	05/15/2007	Systems including packet interfaces, switches, and packet DMA circuits for splitting and merging packet streams	MOLL, LAURENT R.
11933297	Not Issued	25	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
11933319	Not Issued	25	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
11933333	Not Issued	30	10/31/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT R.
12362679	Not Issued	25	01/30/2009	Hypertransport/SPI-4 Interface Supporting Configurable Deskewing	MOLL, LAURENT R.
60731784	Not Issued	159	10/31/2005	Extend cache operations to provide control over which levels of the hierarchy they apply to	MOLL, LAURENT R.
60731969	Not Issued	159	10/31/2005	Instructions giving hints to the hardware prefetcher for more efficient prediction of prefetches	MOLL, LAURENT R.
60736632	Not Issued	159	11/15/2005	Power conservation via DRAM access reduction	MOLL, LAURENT R.
60736736	Not Issued	159	11/15/2005	Small and power-efficient cache that can provide data for background DMA devices while the processor is in a low-power state	MOLL, LAURENT R.
60743560	Not Issued	159	03/20/2006	Prefetch Hardware Efficiency via Prefetch Hint Instructions	MOLL, LAURENT R.
60744592	Not Issued	159	04/10/2006	Improved Prefetch Hardware Efficiency via Prefetch Hint Instructions	MOLL, LAURENT R.
60746049	Not Issued	159	04/30/2006	Reduced Power Cache Memory With Per-Sector Power Control	MOLL, LAURENT R.
60747200	Not Issued	159	05/14/2006	Reduced Power Cache Memory With Per-Sector Power Control	MOLL, LAURENT R.
60747818	Not Issued	159	05/22/2006	Re-Fetching Cache Memory	MOLL, LAURENT R.
60761220	Not Issued	159	01/23/2006	Power conservation via DRAM access reduction	MOLL, LAURENT R.
60761925	Not Issued	159	01/25/2006	Small and power-efficient cache that can provide data for background DMA devices while the processor is in a low-power state	MOLL, LAURENT R.

60803367	Not Issued	159	05/28/2006	Re-fetching Cache Memory	MOLL, LAURENT R.
60804085	Not Issued	159	06/06/2006	Application-Directed Rank Coalescing for Memory Power Management	MOLL, LAURENT R.
09517369	6314156	150	03/02/2000	Space-efficient multi-cycle barrel shifter circuit	MOLL, LAURENT RENE
10821397	7240141	150	04/09/2004	PROGRAMMABLE INTER-VIRTUAL CHANNEL AND INTRA-VIRTUAL CHANNEL INSTRUCTIONS ISSUING RULES FOR AN I/O BUS OF A SYSTEM-ON-A-CHIP PROCESSOR	MOLL, LAURENT RENE
60380740	Not Issued	159	05/15/2002	System on chip for networking	MOLL, LAURENT RENE
09114753	6292762	150	07/13/1998	METHOD FOR DETERMINING A RANDOM PERMUTATION OF VARIABLES BY APPLYING A TEST FUNCTION	MOLL, LAURENT RENE
09763724	6844424	150	02/27/2001	METHOD FOR OBTAINING AVIAN BIOLOGICAL PRODUCTS	MOLLARD, LAURENT
11111886	Not Issued	93	04/22/2005	MOULD FOR NANO-PRINTING, PROCESS FOR MANUFACTURING SUCH A MOULD AND USE OF SUCH A MOULD	MOLLARD, LAURENT
10395505	7275216	150	03/24/2003	SYSTEM AND METHOD FOR DESIGNING ELECTRONIC FORMS AND HIERARCHICAL SCHEMAS	MOLLICONE, LAURENT
10395506	7415672	150	03/24/2003	SYSTEM AND METHOD FOR DESIGNING ELECTRONIC FORMS	MOLLICONE, LAURENT
10459179	7168035	150	06/11/2003	BUILDING A VIEW ON MARKUP LANGUAGE DATA THROUGH A SET OF COMPONENTS	MOLLICONE, LAURENT
10632437	Not Issued	71	08/01/2003	Conversion of structured documents	MOLLICONE, LAURENT
10854961	7281018	150	05/26/2004	FORM TEMPLATE DATA SOURCE CHANGE	MOLLICONE, LAURENT
11072087	Not Issued	71	03/04/2005	Designer-created aspect for an electronic form template	MOLLICONE, LAURENT
11107347	Not Issued	61	04/15/2005	Query to an electronic form	MOLLICONE, LAURENT
11203818	Not Issued	61	08/15/2005	Recognizing data conforming to a rule	MOLLICONE, LAURENT

11320208	7505994	150	12/28/2005	XPATH EXPRESSION BINDING USING XPATH TRACKER WITH DYNAMIC OR STATIC PATH EVALUATION	MOLLICONE, LAURENT
11567133	Not Issued	30	12/05/2006	Building Electronic Forms	MOLLICONE, LAURENT
11567140	Not Issued	30	12/05/2006	Incrementally Designing Electronic Forms and Hierarchical Schemas	MOLLICONE, LAURENT
11567149	Not Issued	30	12/05/2006	Closer Interface for Designing Electronic Forms and Hierarchical Schemas	MOLLICONE, LAURENT

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